Amendment to the Specification

Please replace the paragraph at page 5, line 32, to page 6, line 25 with the following amended paragraph:

Fig. 2A is a cross section of the ESD protection circuit of the present invention, and Figs.2B and 2C are respectively the top view and the equivalent circuit diagram of Fig. 2A. The ESD protection circuit 10 of the present invention is coupled to a pad 12 of an integrated circuit (IC) to protect the core circuit 14 of the IC from ESD event. The ESD protection circuit 10 comprises a p-type semiconductor substrate 16, a n-well 18 and a p-type anode doped region 20. The n-well 18 is formed in the semiconductor substrate 16. The anode doped region 20 is formed in the n-well 18. A gate structure 22 is formed in the substrate 16 outside the n-well 18 and is comprised of a first side 26 and a second side 24. An n-type first doped region 28 is formed between the n-well 18 and the gate structure 22 and is adjacent to the first side 26 of the gate structure 22 in the semiconductor substrate 16. An n-type second doped region 30 is formed in the semiconductor substrate 16 and adjacent to the second side 24 of the gate structure 22 in the semiconductor substrate 16, wherein the first doped region 28 and the second doped region 30 are both heavily doped regions N+ in the present invention, as shown in Fig. 2A. A p-type first contact region 34 and an n-type second contact region 36 are respectively formed in the semiconductor substrate 16 and the n-well 18. As shown in Fig. 2A, the anode doped region 20, the n-well 18, the semiconductor substrate 16 and the second doped region 30 form a PNPN structure. Therefore, the anode doped region 20, the n-well 18, the semiconductor substrate 16 and the second doped region 30 are respectively the anode, anode gate, cathode gate and cathode of a semiconductor control rectifier (SCR) formed by the PNPN structure.